# All Copper Implementation Plan (A Template for Technology Implementation)

**DOCUMENT IDENTIFIER:** A-MN-ELMF733-00-0000 Rev A, 16-Aug-1990

**ABSTRACT:** This document describes the implementation plan for converting printed-wiring board (PWB) manufacturing to an All Copper process.

**APPLICABILITY:** This document applies to all Digital manufacturing sites worldwide and to qualified suppliers.

**STATUS:** APPROVED 16-Aug-1990; use VTX SMC for current status.

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# 1 EXECUTIVE SUMMARY

This document explains the All Copper process, its history, its Printed Wiring Board (PWB) impact, its Module Assembly impact, and the issues that must be addressed when considering the implementation of an All Copper technology.

The goal of the All Copper process is to supply a PWB that gives Module Assembly a competitive advantage in the assembly of fine pitch devices (25 mil and less). With a flatter surface mount component (SMC) attachment surface, a clearer and more recognizable fiducial, and a greater volume consistency of tin/lead (Sn/Pb), it has been shown that first pass process yields increase. The actual percentage increase depends upon the density of the Fine Pitch Surface Mount Technology (FP-SMT).

# 2 INTRODUCTION

This Implementation Plan is aimed at manufacturing and design groups that are contemplating the change of an existing product or the introduction of a new product. Either of these situations affords the opportunity to realize the benefits of All Copper Printed Wiring Board (PWB) technology for Digital.

## 2.1 INTENT

It is the intent of this document to simplify the implementation of the All Copper technology process. To this end, a list of contact persons follows. As questions arise, please contact these individuals.

## 2.2 LIST OF CONTACT PERSONS

**Table 1: Contacts**

| Name | | Node | DTN |
|---|---|---|---|
| Bruce Short | Program Manager | BOARDS::SHORT_B | 226-2076 |
| Paul Thibodeau | Modules | PARITY::THIBODEAU | 247-2355 |
| Pat Dombrowski | Modules | SALEM::DOMBROWSKI | 285-2156 |
| Terri Giversen | Reliability | RELYON::GIVERSEN | 240-6404 |
| Paul Terranova | NRO Labs | FRAGLE::TERRANOVA | 234-4905 |
| Jim Latouche | PWB-GIA | BOARDS::LATOUCHE | 226-2274 |

## 2.3 SCOPE

This document will aid the designer and the manufacturer in the implementation of the All Copper process. All Copper PWB technology can be implemented in all existing designs and in all existing processes that presently use Solder Mask Over Bare Copper (SMOBC) and/or reflowed tin/lead plate PWB technology. The All Copper technology has been shown to be a viable, cost-effective alternative. This cost benefit is derived mainly through quality improvements for fine pitch devices (25 mil) in module assembly.

The production of pitches finer than 25 mil shows promise, and may even prove to be viable only with All Copper. At this date, however, this has yet to be demonstrated.

While modules process compatibility has been proven at several manufacturing sites, each modules' processing manufacturing site has unique processing characteristics, the compatibility of which must be verified. Therefore, each site must perform its own experiments to confirm All Copper compatibility with its particular processes.

When performing these compatibility experiments, particular attention must be paid to the following.

- Fluxes
- Thermal excursions
- Wave solder preheat temperature profiles
- Dwell times
- Cleaning chemistry
- Storage
- Handling procedures

Each of these factors may cause problems in an All Copper process. While All Copper technology is robust, and relatively forgiving of changes in the above process characteristics, failure to confirm compatibility between All Copper and the site's existing process may lead to processing problems, sprcifically solderability. Such problems may cause extensive rework and/or excessive costs. It is with this in mind that process compatibility is required to be confirmed before All Copper implementation. Once confirmed, switching an existing product over to All Copper should be performed gradually.

The All Copper PWB/modules processes mentioned in this plan are qualified through the following manufacturing site testing conditions. Successful modification of these conditions in a module site's existing process may be achieved through additional site compatibility studies at the time of implementation.

1. Desiccant storage of PWBs
2. Visual inspection (pink color) and nitric acid test (BZT presence) confirmed prior to modules processing
3. RMA flux chemistries used throughout the attach processes
4. Careful board-edge handling throughout the modules processes
5. Solvent and/or saponified aqueous cleaning used
6. 8 day dwell - first solvent clean to last solder attach
7. 14 day dwell - first saponified aqueous clean to last solder attach
8. Typical infrared, vapor-phase, and wave-solder processes used

## 2.4 ABSTRACT

The objective of the All Copper Process Program is to develop and introduce the processing of All Copper printed wiring boards within Digital for Fine Pitch Surface Mount Components (FP-SMC).

As finer component lead pitches are used in increasingly tighter circuit patterns, accurate placement and bonding will be increasingly more difficult. A major contributor to this difficulty is the nonplanar surface of typical solder-plated and solder hot air leveled PWBs. An All Copper PWB (no solder on component mounting pads) delivers a very planar surface to the placement operation that makes placement easier and visual inspection more definitive. This results in a more consistent attach process and improved final solder joint quality.

Implementation of the All Copper processes within Digital requires the coordination of PWB fabrication, Module Assembly, and various manufacturing support groups. The All Copper process must be implemented to minimize impact upon present processes, while achieving the benefits of All Copper processing.

This project has developed an All Copper process that uses PWBs fabricated by Digital's internal and external PWB fabrication sites. The fabricated PWBs are then assembled into modules using Digital's module assembly sites and existing equipment and processes. There is a minimum impact to present module processes and equipment, and the process delivers a shippable product to Digital's customers.

Essentially, the All Copper process simplifies the fabricated PWB inspection, the solder paste deposition process, and the component placement process, and it improves the paste reflow process. These improvements result in a more consistent process that yields a better quality fine pitch (25 mil or finer lead pitch) product.

Unfortunately, All Copper is not a panacea for Digital's product cost, module solderability concerns, fine pitch attachment concerns, or reliability enhancement program. However, when All Copper is implemented correctly, it will have a significant and favorable impact in all of these areas, and other areas.

# 3 HISTORY

## 3.1 OLD/NEW TECHNOLOGY

All Copper is not a new technology. It has been used for the past several decades starting with simple, double-sided boards. One of the major protective coatings used at that time was called "Seal-Brite." There is also a benzotriazole complex that IBM has been using for the past 27 years to produce their All Copper PWBs. So All Copper is not a new technology, only an enhancement to an old chemical that other US and Japanese PWB fabricators have been using. Only recently has Digital considered the All Copper technology.

Changes in government/industry climate and in Digital's philosophy have precipitated a new interest in the All Copper PWB technology. Environmental concerns about lead use and lead waste have driven the electronic manufacturer away from tin-lead as a coating for PWBs. Additionally, the electronic industry's trend toward surface mount devices of increasingly finer lead pitch exacerbates the need for more planar PWB mounting surfaces. The nonplanar tin-lead reflowed surface of today's PWBs is easily improved upon by the more planar plated bare copper surface. These two forces are now combined in a Digital product pull, or requirement. New product designers have discovered the benefits of All Copper PWBs. Additionally, All Copper, in conjunction with other emerging technologies (low melt soldering, laser welding), affords the designer and Digital a significant cost reduction by allowing the use of less expensive PWB laminate materials.

### 3.2 WHAT IS ALL COPPER?

An All Copper PWB is a Solder Mask Over Bare Copper (SMOBC) board that has been cleaned and subjected to an anti-oxidant copper chelating agent rather than to Sn/Pb plating or Hot Air Solder Leveling (HASL).

A typical raw board supplied by the PWB fabricator does not have a tin/lead plating, neither under the solder mask nor on the exposed areas. The exposed areas are seen as pink copper protected by an invisible antioxidant complex. In this case, the antioxidant is Benzotriazole (BZT).

**NOTE**

**A stripped reflowed tin/lead or hot air soldered, level PWB SHOULD NOT be used to fabricate an All Copper PWB.**

### 3.3 WHAT IS BENZOTRIAZOLE?

To protect the copper circuitry and holes from oxidation and to allow for good solderability, an inhibitor (an antioxidant) is required. For Digital, this inhibitor has typically been a coating of Sn/Pb, though it could also be an organic compound of nitrogen. When such a compound is applied to the PWB copper surface, the nitrogen's excess electrons bond with the cupric ions on the surface of the PWB, giving it a protective complex. Benzotriazole is a chemical that has a high nitrogen content and therefore forms an effective antioxidation complex with the PWB's copper surface. This complex is approximately 50 angstroms thick, is invisible, and adheres only to copper.

The inhibitor constituent recommended for Digital is a mixture of methyl alcohol (<15%), benzotriazole (<2%), Sodium m-nitrobenzenesulfonate (<2%) and water (>80%). This mixture is manufactured by Enthone Corporation with a trade name of Entex CU-56. However, it is only one of several complexing chemicals that can be used as an antioxidant for PWBs.

## 4 RATIONALE FOR ALL COPPER

The advantages of All Copper PWBs (compared to tin/lead coated PWBs) are as follows.

a. Reliability greatly increased:
   - — No thermal stress from HASL
   - — Surface cleaner - minimum to no migration

b. Greater shelf life - several years instead of six months for Sn/Pb.

c. Greater hole wall uniformity

d. Greater hole to hole size consistency

e. No change in electrical characteristics

f. Greater surface planarity:
   - — Aids uniformity of solder paste
   - — Aids component placement
   - — Significant reduction in solder bridges (FP-SMT)

g. Improvement in fiducial recognition

h. Visual solder paste inspection easier

i. Better solderability

j. PWB and Module process yield improvement

Module Process Yields:

All Copper technology was implemented because of its advantages for assembling fine pitch surface mount components. With a flatter SMC attachment surface, a clearer and more recognizable fiducial, and greater volume consistency of Sn/Pb, first-pass process yields may increase, depending upon the density of FP-SMT.

Value Engineering:

The concepts of value engineering, cost reduction, and cost avoidance play a key role in the consideration of All Copper PWB technology. All Copper PWB costs typically have been quoted as much as 9% lower then equivalent designs using SMOBC technology. However, cost savings vary between PWB vendors and the exact savings, if any, will have to be negotiated.

Design for Manufacture (DFM) Considerations:

The Design for Manufacturability PACE software package cites a material savings for All Copper PWBs.

Environmental Niche:

All Copper PWB fabrication allows for an overall lower use of tin/lead. As such, the operation will be safer, will minimize waste disposal issues, and will simplify regulatory compliance.

Reliability Niche:

The PWB fabrication process of an All Copper board has one less thermal excursion by virtue of the elimination of the Sn/Pb reflow or the hot air level steps in the Sn/Pb plate process or the SMOBC process, respectively. This represents a reliability improvement in the finished module (although this improvement is not measurable).

Also, by nature of the All Copper PWB process itself, the board is comparatively clean when viewed with a microscope. In flowing gas environmental testing, All Copper samples showed minimal copper migration when compared to the same technology samples using Sn/Pb.

# 5 IMPLEMENTATION TEMPLATE

The following is a check list of items that must be addressed when a manufacturing/design site considers All Copper technology implementation. The results of some of these steps will indicate whether implementation should continue. Subsequent subheads in this section define specific concerns that should be understood before implementation.

| ACTIVITY | COMMENTS |
|---|---|
| Process Audit | Possible Determinant; May Point to Areas of Process Adjustment |
| Identify Product | Requires Qualified PWB Vendor |
| Quote Product<br>- Reflowed Plating<br>- SMOBC<br>- All Copper | Possible Determinant to Continuing if Cost PWB Savings Is the Major Criteria |
| Perform Test Vehicle Run of Product From a Digital AC/PWB Qualified Vendor | Possible Determinant; Requires Module Process Compatibility |
| Communicate to Operators | Product Appearance Is Different |
| Communicate to Customers | Product Appearance Is Different |
| Communicate to Site PWB Vendors | Possible Determinant - May Have to be Qualified |
| Communicate to Module Sites Assembling Same Product | Other Sites May Not Be Using All Copper Process |
| Perform Process Compatibility Run | Possible Determinant - Process May Require Adjustments |
| Perform Yield Study | Possible Determinant - Is There a Manufacturing Benefit? |
| Publish Success Report | |

## 5.1 PROCESS COMPATIBILITY AUDIT

The purpose of a process compatibility audit is to prepare the modules' site for processing All Copper PWBs. It is strongly recommended that this audit be performed to avoid implementation and qualification problems. The modules' site process engineers can conduct this audit with consideration of the concerns listed in Section 5.3 to aid in highlighting potential problems. Additionally, Paul Thibodeau of TRG/MPE (See Table 1) is available to conduct a process audit.

### 5.1.1 Audit Procedure

1. The auditor shall tour the module assembly facility from the receiving dock through the modules level final test area, inclusively, and note the following at each stage of the process.
   a. Storage Conditions
      1. Ambient temperatures
      2. Humidity
      3. Air contamination sources and type
      4. Area storage time
      5. Packaging types

6. Package condition
7. Desiccant used

b. Handling Procedures
   1. Tools/equipment used
   2. Hand
      a. Gloves
      b. Bare hands
   3. opportunity for abrasion
      a. PWB to PWB
      b. PWB to equipment

c. Process Parameters
   1. Prebakes
   2. Adhesive cures
   3. Spot mask cures
   4. Reflow operations
   5. Wave solder operations
   6. Repair operations
   7. Cleaning operations
   8. Post-wave assembly operations
   9. Hand (spot) clean operations

Once potential problem areas are identified, they must be monitored to identify their contribution to problems in the process audit PWB run.

### 5.1.2 Process Audit PWB Run

Five PWBs from a known Digital qualified All Copper PWB vendor shall be purchased. These PWBs shall be of an existing etch design for which the module's site has processing parametric data.

The PWBs shall be fully populated to ensure that thermal transfer is typical of the actual assembly process. Processing and handling of the All Copper audit modules can be best achieved by interleaving the All Copper modules into a lot of SMOBC modules and processing the entire group normally.

The quality of the five All Copper modules shall be at least as good as the SMOBC modules when measured with the usual process metrics. If the All Copper modules fail quality metrics, the contributing process parameter(s) shall be adjusted and the audit run repeated.

## 5.2 AVAILABILITY OF PWB VENDOR BASE

There are a number of PWB vendors who have been qualified to supply Digital with All Copper PWB technology. There are also numerous vendors worldwide that have the All Copper PWB process but have neither been requested by Digital to be qualified, nor have they requested qualification. For a complete listing of All Copper vendors contact Jim Ellinger, Manager PWB-GIA qualification office in LJO1 (node BOARDS::ELLINGER).

## 5.3 IMPLEMENTATION CONCERNS

a. WATER SPOTS:

Water spots have proven to be detrimental to All Copper in the form of poor solderability. Water spots seen on incoming All Copper raw PWBs are indications that the fabricator's process is out of control and the product should not be accepted, per DEC STD 176-0 *Printed-Wiring Board Acceptance Criteria*.

The rework for PWBs with water spots is to have the qualified All Copper PWB fabricator reprocess the PWBs through a controlled All Copper process. However, each rework cycle will reduce the amount of copper on the etch and in the hole; the exact amount will depend upon the fabricators microetch cleaning process. On the second and all follow-on rework cycles, the fabricator must show evidence, through cross-sectioning, that the copper required by DEC STD 176 is still in compliance.

b. HANDLING:

The BZT coating is susceptible to damage and/or degradation from three sources: abrasion, excessive humidity, and fingerprints. Digital's present storage and handling specifications are adequate to ensure that the BZT coating integrity will not be compromised.

**CAUTION**

**Though the specifications as written are adequate, compliance to these specifications may be less then complete. Additionally, all handling of the raw PWB prior to stocking in the module assembly site shall be done with double cotton gloves or with finger cots over cotton gloves.**

c. SHELF LIFE:

This was initially an important issue with the development team, but investigation and experimentation demonstrated that the BZT complexed copper surface has a shelf life of two years minimum under normal module storage environments (70±15 °F at RH <80%).

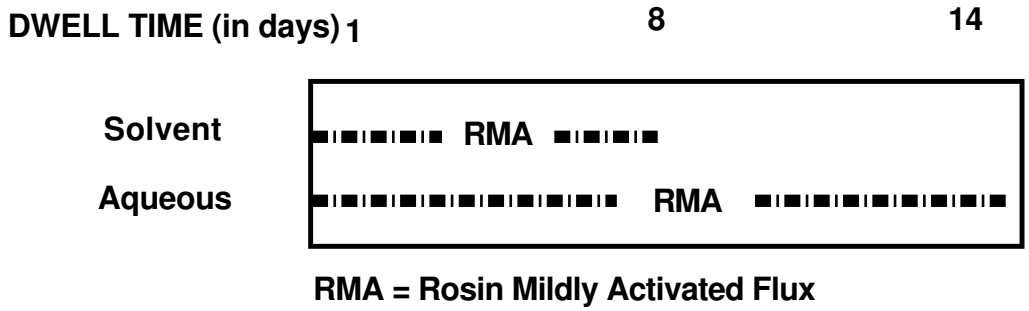
d. PROCESS CLEANING:

It has been proven that the standard temperatures and solvents used in todays module process will not affect the BZT coating; however, saponified water cleaning will affect the coating.

As previously mentioned, aqueous cleaning will attack and reduce the BZT protective coating. Once the coating has been removed, copper oxidation will start to occur and soldering will become more difficult without proper processing techniques.

To properly implement All Copper PWBs into the module SMT process without experiencing soldering difficulties, the following is strongly recommended.

- The maximum dwell time between the initial thermal excursion and cleaning after BZT application and the last soldering process to be done to BZT-protected copper shall be as indicated in the attached chart:




- The dwell times of 8 days and 14 days are the lengths of time between the first clean and the last thermal excursion to achieve solder attachment. These are not maximum allowable dwells; rather, they represent the maximum that has been tested at this time.

  Longer dwells may be achievable and can be established through site compatibility studies.

- POST-WAVE SOLDER ASSEMBLY

  The aqueous clean after wave solder is only a minor concern because, at this time, assembly of the module approaches completion. The type of cleaning (flux) used for rework and for the attachment of components that could not be wave soldered are being addressed. The time delay between wave solder and the next soldering operation is the key factor in determining the amount of cleaning required on an exposed copper area. A few hours will only require the addition of an RMA flux, while heavy oxidation resulting from several days of delay may require the abrasive action of a pink pearl eraser and an RA flux.

## 5.4 COMMUNICATIONS

As in any endeavor, communication among all participants is critical to success. With the implementation of an All Copper technology, special attention must be given to communication between process operators and customers.

### 5.4.1 Customer Awareness

Extensive reliability testing has been conducted on All Copper PWBs, especially in the area of dendritic growth and migration. It has been shown that an All Copper PWB is less prone to failure due to migration than the standard SMOBC PWBs. With the type and amount of reliability testing performed on All Copper PWBs, combined with its wide use and acceptance by other major module users, Digital's standards now allow exposed copper on completed modules. This does not degrade the products reliability nor its expected life cycle.

The site customer, whether Digital or external, should be informed prior to receiving an All Copper module and should be made aware of changes to DEC STD 116 *Workmanship Standards Manual - Introduction*, which allows exposed copper on a finished module. This difference, though not always obvious to the customer, must be addressed proactively to ensure good customer relations. This will avoid erroneous product/module returns for DEC STD 116 "non-compliance" despite the new revision being met.

### 5.4.2 Operator Awareness

All those who handle an All Copper PWB must realize that it is, like all other types of PWBs, susceptible to rough handling, water, finger prints, and other contaminants. Exposure to these types of abuse degrades the solderability of any PWB surface, especially that of All Copper.

With the introduction of All Copper technology into Digital, the appropriate standards have been updated to allow for the shipment of completed modules with exposed copper. For exact definitions on the degree of acceptability, refer to the list of referenced documents in Appendix B.

When there is a need for adding wires or components to a bare copper land area on a completed module, additional flux may be required. Once the All Copper module has been processed, the protective complex may have been removed and oxidation may have started. This is an acceptable condition. However, due to this oxidation, additional flux may have to be added over the limited amount in the solder core to achieve an acceptable solder joint.

There are process and product differences with All Copper modules which will generate questions. If these differences are addressed early and proactively, then fewer questions and doubts will arise. These differences are as follows.

- Pink color of incoming board
- Nitric Acid test
- Glove handling in Incoming Inspection
- Storage with interleaf slats
- Inspection of paste deposition (SMT)
- Visually different surface
- Exposed copper around the joint
- Bare copper pads on finished module
- Water washing
- Dwell times between thermal excursions
- Handling

### 5.4.3 PWB Vendor Awareness

It is necessary for the module manufacturing site to inform its PWB vendors as early as possible of the site's interest in All Copper PWB processing. This may be best accomplished when the request for quote is initiated. Some PWB fabricators have All Copper processing capability; others will have to develop the capability. In either case, early notice that the module site is considering All Copper as a requirement is helpful to the fabricator.

**NOTE**

**Vendors MUST NOT be allowed to use a reflowed tin/lead or hot air solder leveled PWB to fabricate an All Copper PWB.**

## 5.5 COMPATIBILITY

### 5.5.1 Equipment Compatibility

There is NO need for any additional equipment or for any modifications to existing equipment in order to process All Copper PWBs through the module assembly surface mount (single and double sided) and thru-hole lines.

### 5.5.2 Process Compatibility

Before an All Copper PWB is implemented into any module process, be it surface mount or through hole, it first must be established that the existing process is compatible to All Copper. Although an All Copper PWB has good solderability characteristics, it is not to be used in lieu of good (standard) soldering practices and controls. The solderability of an All Copper PWB is affected by the parameters and controls of the process.

While modules process compatibility has been proven at several manufacturing sites, each module's processing manufacturing site has unique processing characteristics, the compatibility of which must be verified. Therefore, each site must perform its own experiments to confirm All Copper compatibility with its particular processes.

When performing these compatibility experiments, particular attention must be paid to the following.

- Fluxes
- Thermal excursions
- Wave solder preheat temperature profile
- Dwell times
- Cleaning chemistry
- Storage
- Handling procedures

Each of the above factors has the potential to cause problems in an All Copper process. While All Copper technology is robust, and relatively forgiving of changes in process parameters, failure to confirm compatibility between All Copper and the site's existing process may lead to processing problems such as poor yield, extensive rework, and/or excessive costs. These potential problems create the requirement that process compatibility must be confirmed before All Copper implementation. Once confirmed, switching an existing product to All Copper should occur gradually.

The existing module assembly surface mount and through hole process, including wave solder, must be in control and yielding good quality product before All Copper PWBs are introduced into the line. Once the standard process has been verified to be in control, the following actions are recommended.

1. Surface Mount PWB
   a. Procure a PWB from a Digital qualified All Copper vendor.
   b. Inspect the All Copper PWB to ensure that the exposed copper areas are of a pink color and show no evidence of water spots.
   c. Subject the All Copper PWB to the surface mount onsertion, reflow, and cleaning process. For this "initial" compatibility study there is no need, depending upon cost, to use the exact number and type of components.
   d. Inspect the All Copper PWB to the standard solderability criteria.
      - If not acceptable, adjust the attachment process and/or notify personnel listed in Table 1. Then repeat steps a through d.
      - If acceptable, proceed to through-hole processing.
2. Through-Hole
   a. Ensure that the flux, preheat temperature, and conveyer speed meet standard process window requirements.
   b. As in the surface mount process, there is no need to insert all the components. Insert enough components to ensure that there will be no change to the thermal profile.
   c. Process the All Copper PWB through the wave solder operation.
      - If not acceptable, adjust wave process and/or notify personnel listed in Table 1. Then repeat steps a through c.
      - If acceptable, process one lot of All Copper PWBs through the entire process ensuring that all quality criteria are met.

Once process compatibility has been determined, the site is ready to process All Copper PWBs.

**NOTE**

**It is recommended that the switch over of standard product to All Copper be done gradually. First, as with the switch over of fused tin/lead PWBs to SMOBC, ECRs and ECOs must be generated and approved. Second, a gradual phase-in allows personnel time to become familiar with All Copper and its subtle differences.**

## 5.6 QUALITY CRITERIA

With the exception of allowing exposed copper on a finished module, all other quality criteria for non All Copper products are applicable.

## 5.7 Testing Procedure for Antioxidant Copper Chelating Agent

**PURPOSE OF TESTING**

To determine the presence of an antioxidant chelating complex on an All Copper PWB.

**EQUIPMENT REQUIRED**

1. Solution of 10% Nitric acid with deionized (D.I.) water
2. Eye dropper
3. 5X glass
4. Two Q-Tips or cotton swabs
5. Safety glasses with side shields
6. Rubber gloves
7. Watch/clock
8. Bottle of Isopropyl Alcohol

**TEST PROCEDURE**

1. Put on gloves and safety glasses.
2. Locate copper area on PWB.
   First choice: Thieving area
   Second choice: Any large non-soldermask copper area (ground planes)
   Third choice: Any non-soldermasked copper area
   Fourth choice: Any SMT pad area.
3. Ensure that the Nitric acid and D.I. water solution is mixed (gently shake the container).
4. Place a drop of the solution onto the selected copper area.
5. After 60 seconds, examine the area under the drop with the 5X glass for evidence of bubbles.
   a. If there are no bubbles, the PWB has been subject to the antitarnish complex and shall be accepted.
   b. If there is evidence of bubbling the PWB lacks adequate antitarnish protection and shall be rejected.
6. After testing, use a clean/dry cotton swab to blot up all testing solution.
7. Wet a second cotton swab with isopropyl alcohol and clean the test area. If a pad with a hole was used as a test site, ensure that the isopropyl alcohol wetted the hole walls.
8. Allow the PWB to air dry.

## 5.8 PACKAGING

The All Copper PWBs remain subject to the packaging requirements specified in DEC STD 176.

There are no changes to the packaging of completed All Copper modules from those used today for standard modules.

**CAUTION**

**It has been noticed that some packaging materials emit a wet chemistry upon contact with a metal surface. This chemistry will contaminate the surface of an All Copper PWB, resulting in poor PWB solderability.**

## 6 IMPACT STATEMENT

Following are the expected impacts to Digital standards.

| | |
|---|---|
| DEC STD 030 Module Manufacturing Standard - Introduction and General Information | No Impact |
| DEC STD 116-0 Workmanship Standards Manual - Introduction | Exposed copper allowed under the following conditions:<br>• Not shorting<br>• Not cosmetically/Aesthetically incorrect<br>• With 3-mil or greater spacing between exposed areas |
| DEC STD 176 Printed-Wiring Board Acceptance Criteria | DEC STDs 176-00, -01, -03, -04, -05 (-05 is the new All Copper section) |
| DEC STD 265 Module Rework and Repair Standard Procedures | No Impact |
| EL-MF417-01, Surface Mount Technology Reference Manual | No Impact |

# 7 DEFINITIONS - WORDS AND PHRASES

| | |
|---|---|
| All Copper Process | The process of fabricating a printed circuit board without Sn/Pb fusing or hot air soldering leveling, which results in a finished board absent of any solder coating. |
| Benzotriazole (BZT) | The complexing material used to retard Copper oxidation in the All Copper PWB Process. |
| Substrate Material | The material from which the raw PWB is fabricated from: that is, FR-4, polyimide, BT, and so forth. |
| Printed Circuit Board/Printed-Wire Board (PWB) | A substrate upon which various conductive circuit patterns are formed and connected from layer to layer by conductive holes. |
| Circuit Pattern | The electrically conductive copper paths on the surface and inner layers of a printed circuit board. The circuit pattern is frequently characterized or described by its smallest line width and/or line spacing (for example, 25 mil circuitry) |
| Hot Air Solder Level (HASL) | The printed circuit board fabrication process in which molten solder is deposited on the board surface and then the excess blown off with high pressure air. |
| Tin/Lead Plating (Sn/Pb) | The PWB fabrication process characterized by the plating of solder (tin-lead) on all exposed copper areas. |
| Solder Mask Over Bare Copper (SMOBC) | A PWB which has been stripped of its Sn/Pb before solder mask application. After solder mask application, the PWB is subjected to HASL and all exposed copper areas are coated with Sn/Pb. |
| Cross Section | The cutting of a sample, either horizontally or vertically, for the purpose of analyzing its inner structure. |
| Electro-migration | The defect mode characterized by the growth of electrically conductive paths under electrical bias in the presence of contamination and humidity. |
| Module | An assembly of various electrical components onto a printed wiring board. |
| Fine Pitch | Component lead spacing or conductor path spacing of 25 mils or smaller. |
| Lead Pitch | The center to center distance of the leads of a component. |
| Lead Planarity | The property of component leads such that their tips lie in the same plane. |
| Photo Micrograph | A photograph of a microscopic view of a solder joint, usually of a cross section. |
| Pull/Peel | A reliability test procedure which measures the forces characteristic of lead pull/peel as the solder joint parts are separated. |
| Surface Planarity | The characteristic of a substrate foot print that is demonstrated by the ability of individual pads to exist in the same place. |
| Solder Paste | The suspension of finely powdered solder in a mixture of flux and additive to produce a paste-like material which can be screened or stenciled onto a substrate in preparation for component placement and attachment. |
| Solder Joint | The joining of two or more metallic components with molten solder. |
| Surface Insulation Resistance (SIR) | A defect mode characterized by a degradation of surface insulation resistance in the presence of electrical bias and various flowing gases. |
| Product Pull | The requirement of a product line business manager for a technology. The business manager will support this requirement with funding for technological development and application. |
| Paste Reflow | The process of elevating the temperature of solder paste in order to reflow (make molten) the solder and thus make a solder joint. |

# APPENDIX A QUESTIONS AND ANSWERS

## A.1 SOME TYPICAL ALL COPPER QUESTIONS

1. *Plants and Processes:*
2. 
   a. *Which plants have conducted All Copper Experiments?*

      Under the All Copper Program, experiments were performed at the following sites.

      — Salem (NIO)

      — Westfield (WFO)

      — Singapore (ZGO)

      — Maynard Surface Mount Lab

   b. *What products and processes were used?*

      The All Copper Program was divided into two phases.

      Phase I: Single-sided SMT with through-hole (wave solder)
      Phase II: Double-sided SMT with through-hole (localized solderpot)

      The products which were used were

      VAXstar Module for Phase I
      Calypso Memory Module (OPUS) for Phase II

      Figures 1 and 2 show the process flow in each phase and describe the equipment and chemistries used in the evaluation.

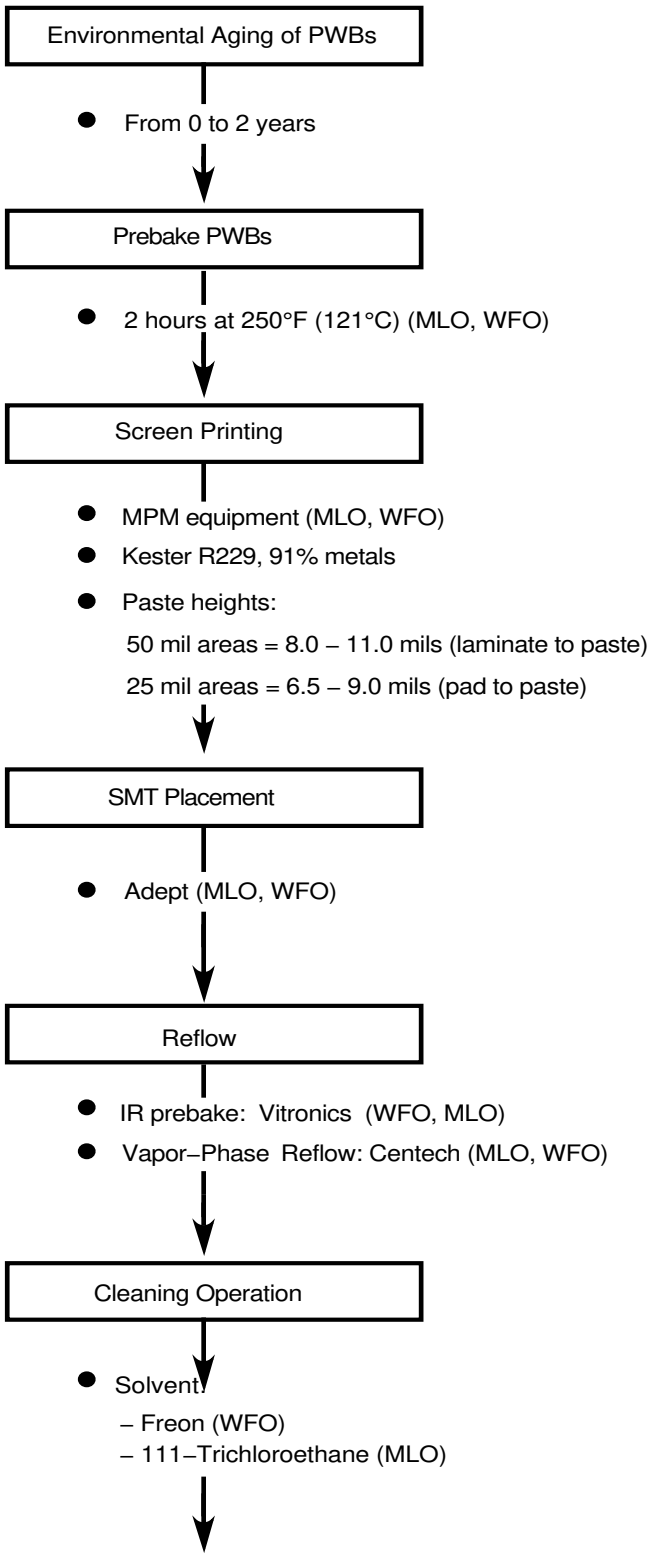
      **NOTE**

      **In Figures 1 and 2, site locations are indicated with their three-character location code.**

   c. *What changes in material handling were required? Were there any significant effects of "poor handling" notices?*

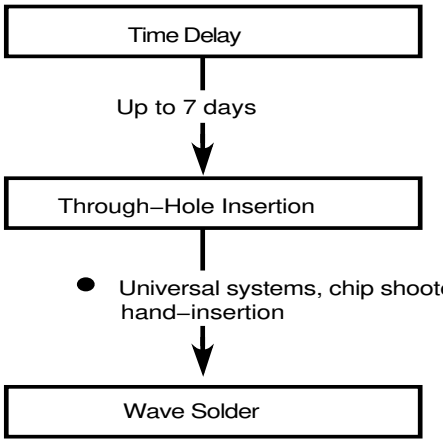
      Poor handling was treated as a variable in many of the experiments conducted in the Phase I and Phase II All Copper projects. There were no significant effects noted between the quality of clean boards versus heavily fingerprinted boards. However, it is recommended that All Copper boards be handled by the edges only, as is specified for tin/lead boards.

**Figure 1: PHASE I: VAXstar Module**


Environmental Aging of PWBs
From 0 to 2 years
Prebake PWBs
2 hours at 250°F (121°C) (MLO, WFO)
Screen Printing
MPM equipment (MLO, WFO)
Kester R229, 91% metals
Paste heights:
50 mil areas = 8.0 – 11.0 mils (laminate to paste)
25 mil areas = 6.5 – 9.0 mils (pad to paste)
SMT Placement
Adept (MLO, WFO)
Reflow
IR prebake: Vitronics (WFO, MLO)
Vapor–Phase Reflow: Centech (MLO, WFO)
Cleaning Operation
Solvent:
– Freon (WFO)
– 111–Trichloroethane (MLO)

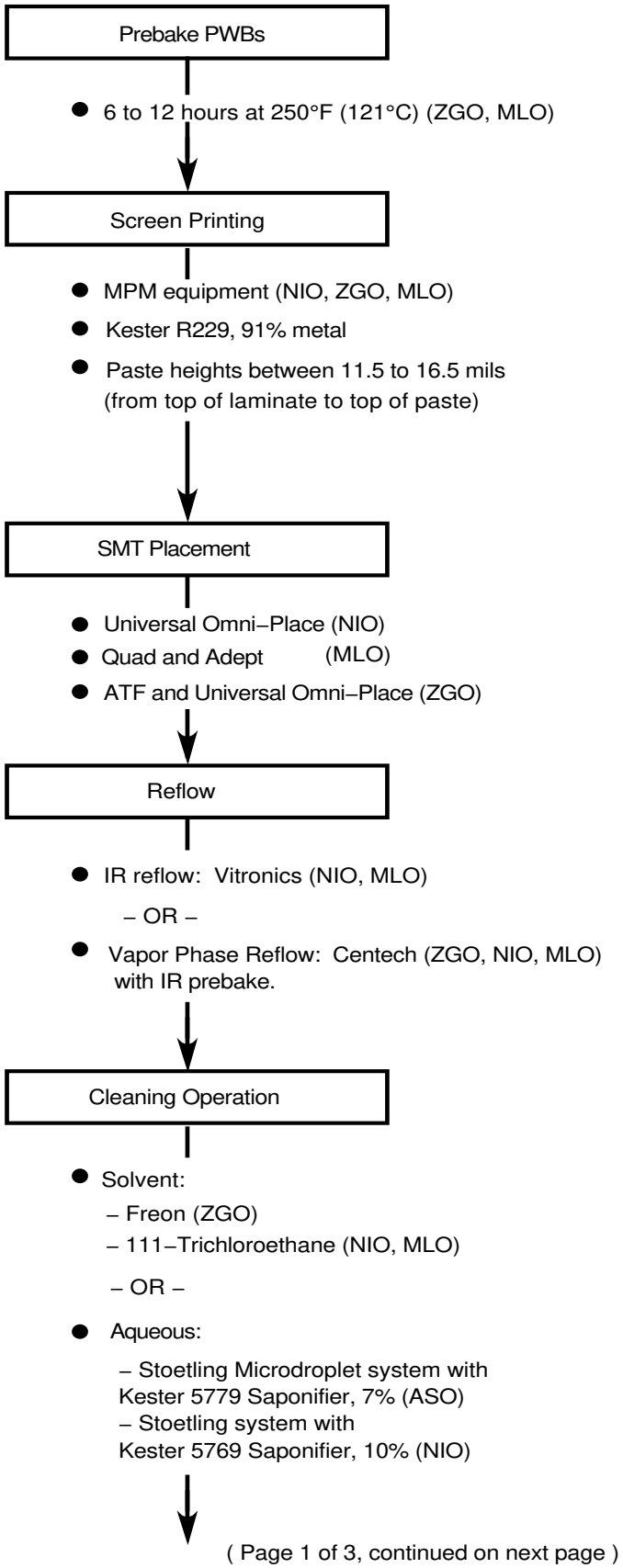
( Page 1 of 2, continued on next page )

**Figure 1: PHASE I: VAXstar Module, continued**



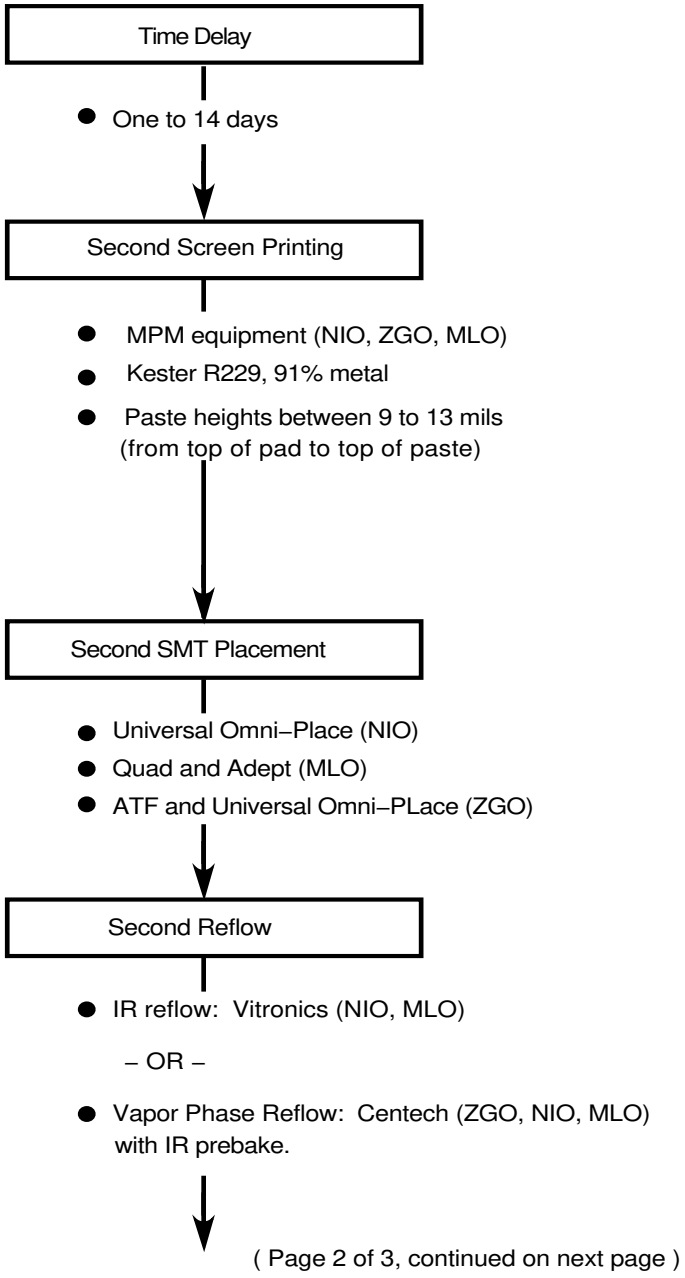

( 2 of 2 )

**Figure 2: PHASE II: Calypso Memory Module (OPUS)**


Prebake PWBs
6 to 12 hours at 250°F (121°C) (ZGO, MLO)
Screen Printing
MPM equipment (NIO, ZGO, MLO)
Kester R229, 91% metal
Paste heights between 11.5 to 16.5 mils
(from top of laminate to top of paste)
SMT Placement
Universal Omni–Place (NIO)
Quad and Adept (MLO)
ATF and Universal Omni–Place (ZGO)
Reflow
IR reflow: Vitronics (NIO, MLO)
– OR –
Vapor Phase Reflow: Centech (ZGO, NIO, MLO)
with IR prebake.
Cleaning Operation
Solvent:
– Freon (ZGO)
– 111–Trichloroethane (NIO, MLO)
– OR –
Aqueous:
– Stoetling Microdroplet system with
Kester 5779 Saponifier, 7% (ASO)
– Stoetling system with
Kester 5769 Saponifier, 10% (NIO)

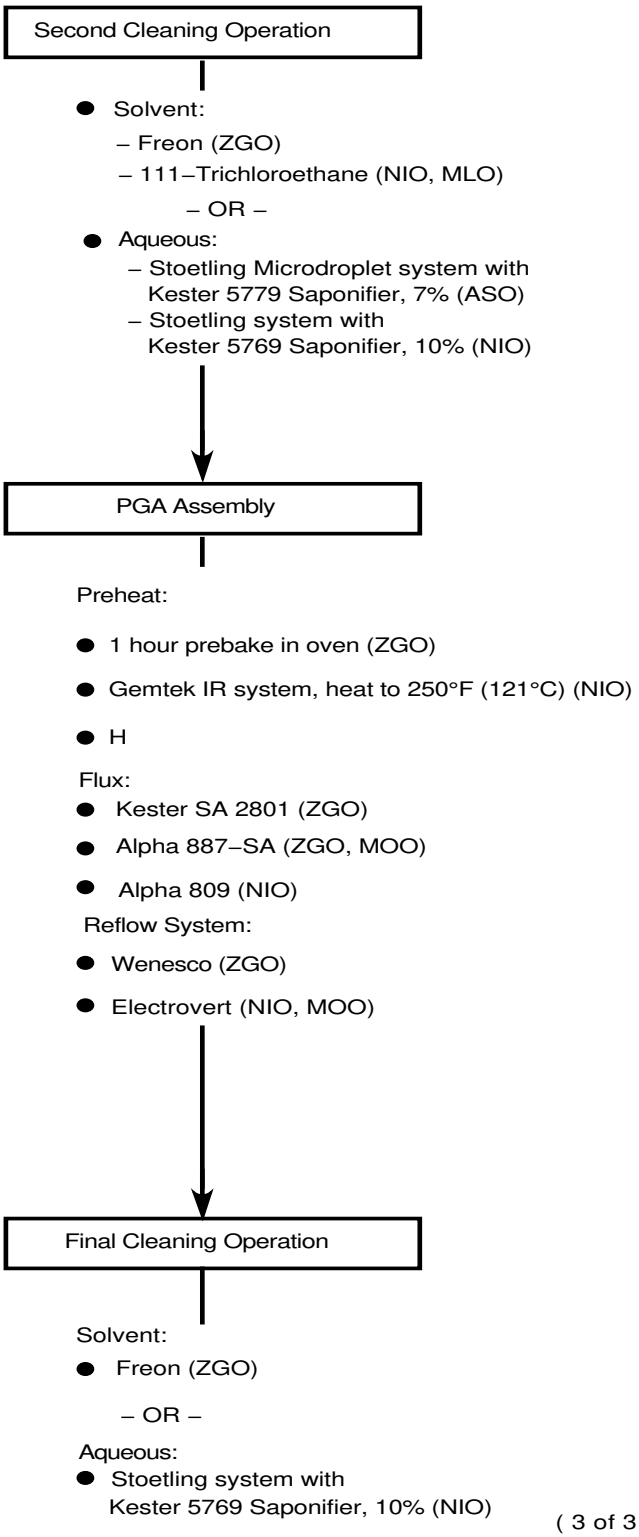
( Page 1 of 3, continued on next page )

**Figure 2: PHASE II: Calypso Memory Module (OPUS), continued**


Time Delay
One to 14 days
Second Screen Printing
MPM equipment (NIO, ZGO, MLO)
Kester R229, 91% metal
Paste heights between 9 to 13 mils
(from top of pad to top of paste)
Second SMT Placement
Universal Omni–Place (NIO)
Quad and Adept (MLO)
ATF and Universal Omni–PLace (ZGO)
Second Reflow
IR reflow: Vitronics (NIO, MLO)
– OR –
Vapor Phase Reflow: Centech (ZGO, NIO, MLO)
with IR prebake.

( Page 2 of 3, continued on next page )

**Figure 2. PHASE II: Calypso Memory Module (OPUS), continued**




( 3 of 3 )

3. *What were the results in Phase I, and were they supported by detailed analysis of solder joint integrity, that is*

   *Microsectional analysis*
   *SEM*
   *Pull/Peel*
   *Solderability*
   *Accelerated aging?*

   PHASE I:

   The results of the Phase I study were published in June, 1989. The full report *Phase I: All Copper Characterization Report*, (available upon request from Pat Dombrowski, see Table 1) covers all the variables listed in the Phase I flow diagram. The report is based on 100% visual inspection, microsections, and pull/peel strength measurements of the solder joints. Approximately 100 VAXstar modules were assembled for this evaluation in both lab and volume production environments. In general, the evaluation found the All Copper PWB to produce solder joints of equal quality to the SMOBC PWB. In addition, there was a substantial improvement in the number of solder short defects on the All Copper PWB.

   Accelerated aging was tested in Phase I. All Copper boards were aged to an equivalent shelf life of 2 years then assembled. There was no significant difference in solder joint integrity between the two year modules assembled and fresh ones.

   PHASE II:

   The results of the Phase II study were published in July, 1990. The processes and variables tested are shown in the Phase II flow diagram. Again, 100% visual inspection, microsections and pull strength data were used to evaluate the solder joints. In this phase of the study, approximately 60 OPUS modules were assembled in volume production environments.

   Briefly, the solder joints formed on the All Copper board were of the same quality as those formed on a tin/lead board. This was for both aqueous cleaning and solvent cleaning, and for both IR and Vapor phase reflow.

4. *What is the mechanism that actually removes the BZT complex from the copper surface?*

   ESCA studies have been performed on the Enthone coating thickness at each step of the double-sided assembly process.

   The thickness of the Cu-56 coating on a fresh board was measured as approximately 30 Angstroms. After the first heat excursion, IR reflow, the coating was so thin as to not be distinguishable from atmospheric contamination. However, after the following sequence of process steps, the oxide formation only measured 40 Angstroms.

   1. IR Reflow
   2. Aqueous Clean
   3. 14 day wait
   4. IR Reflow
   5. Aqueous Clean

5. *What are the estimated dwell times after initial "thermal excursion"?*

   We have tested the following dwell times with no solderability concerns.

   - Up to 8 days after first SMT with Solvent Clean
   - Up to 14 days after first SMT with Aqueous Clean.

   These are the only dwell times tested because of scheduling issues for the experiment. These limits may be exceeded without a solderability problem. However, we have no data to prove it is feasible or not.

6. *Where do water spots occur?*

   Water spots in the assembly process could be produced by improper drying at the end of the aqueous cleaning operation.

7. *Why is the testing in Question 2 above not specified in the All Copper Implementation Plan (Template)?*

   The Implementation Document is not a justification document. It is a follow-on document to other documents that give all testing and associated data used for qualifying All Copper. The Implementation Document has been written as a guideline for Module Manufacturing. Each module site has its own method and equipment for processing a module. There are certain precautions that should be understood and taken by the Module Site to ensure a successful transition to All Copper, which is the reason for the Implementation document.

# APPENDIX B REFERENCED DOCUMENTS

## B.1 EL-Class Digital Documents

| EL-Class Number | Document Title |
|---|---|
| EL-00030-00 | *DEC STD 030-0 Module Manufacturing Standard - Introduction and General Information* |
| EL-00116-00 | *DEC STD 116-0 Workmanship Standards Manual - Introduction* |
| EL-00176-00 | *DEC STD 176-0 Printed-Wiring Board Acceptance Criteria* |
| EL-00265-00 | *DEC STD 265-0 Module Rework and Repair Standard Procedures* |
| EL-MF417-01 | *Surface Mount Technology Reference Manual - 2 Volume Set* |

Use VTX SMC to order copies of EL-class documents from Standards and Methods Control. Send distribution questions to JOKUR::SMC or call DTN: 234-4423.

# APPENDIX C RELATED DOCUMENTS

## C.1 EL-Class Digital Documents

| EL-Class Number | Document Title |
|---|---|
| EL-00084-00 | *DEC STD 084-0 Process and Technology Phase Review Procedure* |
| EL-00088-00 | *DEC STD 088-0 Qualification Procedure for All Printed-Wiring Board Suppliers* |
| EL-00176-01 | *DEC STD 176-1 Printed-Wiring Board Repair Criteria* |
| EL-00176-03 | *DEC STD 176-3 Printed-Wiring Board Acceptance Criteria for SMOBC (Soldermask Over Bare Copper) Product* |
| EL-00176-04 | *DEC STD 176-4 Surface Mount Printed-Wiring Board Acceptance Criteria* |
| EL-00176-05 | *DEC STD 176-5 Printed-Wiring Board Acceptance Criteria for All Copper Product* |
| EL-MF500-00 | *Method of Determining the Solderability of Surface Mountable Packages* |
| EL-MF596-00 | *Modules Process Qualification Procedure and Assessment Checklist* |

Use VTX SMC to order copies of EL-class documents from Standards and Methods Control. Send distribution questions to JOKUR::SMC or call DTN: 234-4423.

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